

Appl. No. 10/072,855
Reply to Office Action of May 14, 2003

Attorney Docket No. 81751.0026

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Amended) A semiconductor device comprising:

a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of a first driver transistor;

a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of a second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and

wherein a width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor.

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2. (Original) The semiconductor device according to claim 1, wherein a width of the second gate-gate electrode layer in the second load transistor is larger than the width of the second gate-gate electrode layer in the second driver transistor.

3. (Original) The semiconductor device according to claim 1, comprising a first adjacent memory cell which is located adjacent to a side of the memory cell where the first gate-gate electrode layer is provided,

wherein the first adjacent memory cell includes a third gate-gate electrode layer having a gate electrode of a third load transistor and a gate electrode of a third driver transistor,

wherein the first load transistor and the third load transistor commonly use a first impurity layer as a source region,

wherein a first contact section is provided on the first impurity layer, and

wherein the first contact section is provided in a region other than a region between the first gate-gate electrode layer and the third gate-gate electrode layer.

4. (Original) The semiconductor device according to claim 1, comprising a second adjacent memory cell which is located adjacent to a side of the memory cell where the second gate-gate electrode layer is provided,

wherein the second adjacent memory cell includes a fourth gate-gate electrode layer having a gate electrode of a fourth load transistor and a gate electrode of a fourth driver transistor,

wherein the second load transistor and the fourth load transistor commonly use a second impurity layer as a source region,

wherein a second contact section is provided on the second impurity layer, and

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wherein the second contact section is provided in a region other than a region between the second gate-gate electrode layer and the fourth gate-gate electrode.

5. (Original) The semiconductor device according to claim 1, wherein the first drain-gate wiring layer is electrically connected to the second drain-drain wiring layer through a contact section, and

wherein the second drain-gate wiring layer is electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

6. (Original) The semiconductor device according to claim 1, wherein the first drain-gate wiring layer is located in a layer lower than the second drain-gate wiring layer.

7. (Original) The semiconductor device according to claim 1, wherein the first drain-gate wiring layer is located in a layer in which the first gate-gate electrode layer is provided.

8. (Original) The semiconductor device according to claim 1, wherein the second drain-gate wiring layer is formed across a plurality of layers.

9. (Original) The semiconductor device according to claim 8, wherein the second drain-gate wiring layer includes a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and

wherein the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer.

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10. (Original) The semiconductor device according to claim 9, wherein the upper layer is electrically connected to the lower layer through a contact section.

11. (Original) The semiconductor device according to claim 9, wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer, wherein the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer, and wherein the upper layer is located in a third conductive layer.

12. (Original) The semiconductor device according to claim 1, wherein the second conductive layer is a nitride layer of a refractory metal.

13. (Original) The semiconductor device according to claim 1, wherein the second conductive layer has a thickness of 100 nm to 200 nm.

14. (Previously Amended) A memory system provided with the semiconductor device defined in claim 1.

15. (Previously Amended) An electronic apparatus provided with the semiconductor device defined in claim 1.